UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,373	01/14/2004	Kazumi Hara	9319I-000647	3618

27572 7590 04/05/2007
HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,373	HARA	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-8, 19-22, 34 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-8, 34 and 42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Serial Number: 10/757373 Attorney's Docket #: 93191-000647
Filing Date: 1/14/2004; claimed foreign priority to 1/15/2003

Applicant: Hara et al.

Examiner: Alexander Williams

Applicant's Appeal Brief filed 1/30/07 has been acknowledged.

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Applicant's Amendment filed 9/22/06 to the election with traverse of species I (claims 5-8, 19-22, 34 and 42), filed 11/22/05, has been acknowledged.

Claims 1-4, 9-18, 23-33, 35-41 and 43-70 have been cancelled.

The disclosure is objected to because of the following informalities: Related application information should be cited and updated.

Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Initially, it is noted that the 35 U.S.C. § 103 rejection based on an insulating layer, a first section of the insulating layer and a second portion of the insulating layer deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 5-8, 34 and 42 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Siniaguine (U.S. Patent Application Publication # 2002/0084513 A1).

5. Siniaguine (figures 1 to 13) specifically figure 8 show a semiconductor chip **104** comprising:

a semiconductor substrate **110**;

an integrated circuit, at least a part of the integrated circuit being formed in the semiconductor substrate;

a penetrating electrode **160** which is formed in a through-hole the semiconductor substrate from

a first surface to a second surface of the semiconductor substrate, the through-hole having sidewalls entirely orthogonal to the first and second surface, and the penetrating electrode having a projection which projects from the second surface; and

an insulating layer **140** formed over an entire surface of the second surface of the substrate, the insulating layer including a first insulating section **(inner portion of 140)** formed in a region that surrounds the projection such that the projection forms a through-bore in the first insulating section above the second surface of the substrate, and he first insulating section being connected to the second insulating section by a radially tapering arcuate portion **(portion of 140 extended past the surface of 110 that the 160 extend out from)** having a varying radius of curvature from the through-bore to the second insulating section, but Siniaguine's figure 8 fail to explicitly show a second insulating section that covers a remaining region of the second surface of the semiconductor substrate; wherein the second insulating section is formed to be thinner than a thickest area of the first insulating section.

Siniaguine's figures 10-12 is cited for showing other embodiments with an insulating section that cover a remaining region of the second surface of the semiconductor substrate. Specifically, Siniaguine's figure 12 discloses show a semiconductor chip **104** comprising:

a semiconductor substrate **110**;

an integrated circuit, at least a part of the integrated circuit being formed in the semiconductor substrate;

a penetrating electrode **160** which is formed in a through-hole the semiconductor substrate from

a first surface to a second surface of the semiconductor substrate, the through-hole having sidewalls entirely orthogonal to the first and second surface, and the penetrating electrode having a projection which projects from the second surface; and

an insulating layer **710,140** formed over an entire surface of the second surface of the substrate, the insulating layer including a first insulating section **(inner portion of 140 that extends past the surface of 110 in which the 160 extends from)** formed in a region that surrounds the projection such that the projection forms a through-bore in the first insulating section above the second surface of the substrate and a second insulating section **710** that covers a remaining region of the second surface of the semiconductor substrate; wherein the second insulating section is formed to be thinner than a thickest area of the first insulating section for the purpose of becoming less likely to detach from the contact if the contact is pulled sideways.

6. The semiconductor chip as defined in claim 5, Siniaguine show wherein the first insulating section is formed so that a thickness of the first insulating section decreases as a distance from the projection increases (fsee figure 8).

7. The semiconductor chip as defined in claim 5, Siniaguine show wherein the projection is formed to have a height higher than a height of a thickest area of the insulating layer (see figure 10).

8. The semiconductor chip as defined in claim 5, Siniaguine show wherein the projection is formed to have a height equal to a height of a thickest area of the insulating layer.

34. Siniaguine show a circuit boardon which the semiconductor chip as defined in claim 5.

42. Siniaguine show an electronic instrument comprising the semiconductor chip as defined in claim 5.

Therefore, it would have been obvious to one of ordinary skill in the art to use the insulating layer, first section of the insulating layer and the section of the insulating layer as "merely a matter of obvious engineering choice" as set forth in the above case law.

Therefore, it would be obviousl to one of ordinary skill in the art to use Siniaguine's figure 10 showing an insualting layer covering second surface entirely by a first insulation portion and a second insulating portion covering the remainer entire portion of the second surface to modify Siniaguine's figure 8 surface with a first insulation portion greater than the second portion and the second portion covering the entire surface for the purpose of providing it would be less likely to detach from the contact if the contact is pulled sideways.

Claims 19-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Siniaguine (U.S. Patent Application Publication # 2002/0084513 A1) in view of Patti (U.S. Patent Application Publication # 2004/0048459 A1).

19. Siniaguine (figures 1 to 13) specifically figure 8 show a semiconductor chip **104** comprising:

a semiconductor substrate **110**;

an integrated circuit, at least a part of the integrated circuit being formed in the semiconductor substrate;

a penetrating electrode **160** which is formed in a through-hole the semiconductor substrate from

a first surface to a second surface of the semiconductor substrate, the through-hole having sidewalls entirely orthogonal to the first and second surface, and the penetrating electrode having a projection which projects from the second surface; and

an insulating layer **140** formed over an entire surface of the second surface of the substrate, the insulating layer including a first insulating section **(inner portion of 140)** formed in a region that surrounds the projection such that the projection forms

a through-bore in the first insulating section above the second surface of the substrate, and he first insulating section being connected to the second insulating section by a radially tapering arcuate portion **(portion of 140 extended past the surface of 110 that the 160 extend out from)** having a varying radius of curvature from the through-bore to the second insulating section, but Siniaguine's figure 8 fail to explicitly show a second insulating section that covers a remaining region of the second surface of the semiconductor substrate; wherein the second insulating section is formed to be thinner than a thickest area of the first insulating section.

Siniaguine's figures 10-12 is cited for showing other embodiments with an insulating section that cover a remaining region of the second surface of the semiconductor substrate. Specifically, Siniaguine's figure 12 discloses show a semiconductor chip **104** comprising:

a semiconductor substrate **110**;

an integrated circuit, at least a part of the integrated circuit being formed in the semiconductor substrate;

a penetrating electrode **160** which is formed in a through-hole the semiconductor substrate from

a first surface to a second surface of the semiconductor substrate, the through-hole having sidewalls entirely orthogonal to the first and second surface, and the penetrating electrode having a projection which projects from the second surface; and

an insulating layer **710,140** formed over an entire surface of the second surface of the substrate, the insulating layer including a first insulating section **(inner portion of 140 that extends past the surface of 110 in which the 160 extends from)** formed in a region that surrounds the projection such that the projection forms a through-bore in the first insulating section above the second surface of the substrate and a second insulating section **710** that covers a remaining region of the second surface of the semiconductor substrate; wherein the second insulating section is formed to be

thinner than a thickest area of the first insulating section for the purpose of becoming less likely to detach from the contact if the contact is pulled sideways.

Siniaguine fails to explicitly show a plurality of integrated circuits, at least a part of each of the integrated circuits being formed in the semiconductor substrate; a plurality of penetrating electrodes each of the penetrating electrodes being formed through the semiconductor substrate from a first surface to a second surface of the semiconductor substrate and having a projection which projects from the second surface.

Patti is cited for showing a interlocking conductor method for bonding wafers to produce stacked integrated circuits. Specifically, Patti (figures 1 to 12) specifically figure discloses interlocking substrates with depressions formed corresponding to IC devices, whereby disclosing a plurality of integrated circuits, at least a part of each of the integrated circuits being formed in the semiconductor substrate; a plurality of penetrating electrodes each of the penetrating electrodes being formed through the semiconductor substrate from a first surface to a second surface of the semiconductor substrate and having a projection which projects from the second surface for the purpose of providing protruding contact structures to interconnect IC components on a wafer.

20. The semiconductor wafer as defined in claim 19, the combination of Siniaguine and Patti show wherein each of the first insulating sections is formed so that a thickness of each of the first insulating sections decreases as a distance from the projection increases.

21. The semiconductor wafer as defined in claim 19, the combination of Siniaguine and Patti show wherein the projection is formed to have a height higher than a height of a thickest area of the insulating layer.

22. The semiconductor wafer as defined in claim 19, the combination of Siniaguine and Patti show wherein the projection is formed to have a height equal to a height of a thickest area of the insulating layer.

Therefore, it would be obvious to one of ordinary skill in the art to use Patti's plurality of integrated circuits and penetrating electrodes and to use Siniaguine's figure 10 showing an insualting layer covering second surface entirely by a first

insulation portion and a second insulating portion covering the remainer entire portion of the second surface to modify Siniaguine's figure 8 surface with a first insulation portion greater than the second portion and the second portion covering the entire surface for the purpose of providing protruding contact structures to interconnect IC components on a wafer for the purpose of providing it would be less likely to detach from the contact if the contact is pulled sideways.

Therefore, it would have been obvious to one of ordinary skill in the art to use the insulating layer, first section of the insulating layer and the section of the insulating layer as "merely a matter of obvious engineering choice" as set forth in the above case law.

Response

Applicant's arguments filed 9/22/06 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 1 and 19 filed 9/22/06" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. ∋ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. ∋ 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL

EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. ə 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/773,774,700-703,758,751,778,734, 737,738,777, 685, 686,680,678,687,696,698,690-693,668,621,730,e23.011,e25.013	1/31/05 7/20/06 3/31/07
Other Documentation: foreign patents and literature in 257/773,774,700-703,758,751,778,734, 737,738,777, 685, 686,680,678,687,696,698,690-693,668,621,730,e23.011,e25.013	1/31/05 7/20/06 3/31/07
Electronic data base(s): U.S. Patents EAST	1/31/05 7/20/06 3/31/07

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1236. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
3/31/07